

We claim:

1. A method for making a heterojunction bipolar transistor, comprising:
(a) depositing a first polysilicon layer over shallow trench regions
and a single crystalline SiGe intrinsic base region over a collector region;

(b) forming an oxide layer over the first polysilicon layer;
(c) forming a first nitride layer over the oxide layer;
(d) etching an opening through the first nitride layer, said opening
corresponding to an emitter opening of said transistor;

(e) filling said emitter opening with a second polysilicon layer;
(f) forming an emitter pedestal from the second polysilicon layer
and the first nitride layer, said emitter pedestal having a width which is wider than
said emitter opening; and

(g) implanting source/drain implant regions into at least the first
polysilicon layer, said source/drain implant regions being self-aligned with the
second polysilicon layer in said emitter pedestal.

2. The method of claim 1, wherein the second polysilicon layer is in the
shape of a T, with respective portions overlapping the first nitride layer.

3. The method of claim 2, wherein said step of forming said emitter
pedestal includes making a length of the first SiGe polysilicon layer on one side of

3 said emitter pedestal and a length of the first SiGe polysilicon layer on another side
4 of said emitter pedestal to be different lengths, and wherein the side with large length
5 will be used as base contact.

1 4. The method of claim 1, wherein the first polysilicon layer is an SiGe
2 layer.

1 5. The method of claim 4, wherein said SiGe layer is less than 0.15 μ m
2 thick.

1 6. The method of claim 1, wherein said oxide layer is a high-pressure
2 thermal oxide layer.

1 7. The method of claim 1, wherein said collector region is an n- epitaxy
2 region on top of a sub-collector region.

1 8. The method of claim 1, wherein said step of forming said emitter
2 pedestal includes making a length of the second polysilicon layer on one side of said
3 emitter pedestal at least substantially equal to a length of the second polysilicon layer
4 on another side of said emitter pedestal, said substantially equal lengths causing said
5 transistor to have equal base resistances on said one side and said another side of said
6 emitter pedestal.

7 9. The method of claim 1, wherein said source/drain implant regions are
8 extrinsic base regions.

1 10. The method of claim 1, wherein said step of forming said emitter
2 opening includes:

3 forming a TEOS layer over the first nitride layer;

4 forming an ARC layer over the TEOS layer;

5 forming a resist over the ARC layer;

6 developing the resist layer and forming patterns on the ARC layer;

7 etching through selective portions of the ARC layer and the TEOS
8 layer; and

9 stripping the resist and ARC layers, wherein the TEOS layer is a hard
10 mask to etch the nitride layer to form said emitter opening.

1 11. The method of claim 1, wherein said step of forming said emitter
2 pedestal includes:

3 forming a second nitride layer over the second polysilicon layer;

4 forming a photoresist over the second nitride layer; and

5 etching away the second nitride layer, the second polysilicon layer,
6 and the oxide layer except in a region underlying said photoresist.

1
Sub
C4

12. The method of claim 11, further comprising:
varying photo tolerance during said step of forming said emitter
pedestal to minimize mis-alignment between the second polysilicon layer in said
emitter pedestal and said emitter opening.

1
SUB
A1

13. A heterojunction bipolar transistor, comprising:
a collector region;
a SiGe base region;
an emitter stack overlying said collector region, said emitter stack
including an emitter opening filled with T-shaped polysilicon, said T-shaped
polysilicon overlying nitride regions included in said stack; and
extrinsic base regions arranged on respective sides of said emitter
stack, said extrinsic base regions being aligned with said emitter polysilicon region
but not being directly aligned with said emitter opening.

1
Sub
C4

14. The transistor of claim 13, wherein said extrinsic base regions are
made from SiGe polysilicon.

1
SUB
A2

15. The transistor of claim 13, wherein one of said extrinsic base regions
is longer than another of said extrinsic base regions, and wherein a base contact is
formed on the longer extrinsic base region.

Sub 4

- 1 16. The transistor of claim 13, wherein said reach-through collector
2 region, emitter stack, and extrinsic base regions are contacted using mid-end-of-line
3 collector, emitter, and base contact contacts respectively.
-

20250726 15:33:50